

CLAIMS

[0054] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image sensor comprising:
a pixel comprising a photosensitive region;
an isolation region adjacent said pixel; and
an isolation gate provided over said isolation region.
2. The sensor of claim 1 wherein said pixel further comprises
at least one transistor gate for transferring photoelectric
charges from said photosensitive region and wherein said
isolation gate is of the same conductivity type as said at least
one transistor gate.
3. The sensor of claim 1 wherein said photosensitive region,
comprises a p-type conductivity substrate, an n-type
conductivity photodiode region, and a p-type conductivity
surface region.
4. The sensor of claim 3 wherein said isolation gate extends
over at least a portion of a region between said
photosensitive region of said pixel and said isolation region
and said isolation gate is biased to accumulate holes in said
region between said photosensitive region of said pixel and
said isolation region.

5. The sensor of claim 3 wherein said isolation gate is biased to expand a region between said photosensitive region of said pixel and said isolation region.
6. The sensor of claim 1 wherein said isolation gate is biased to ground.
7. The sensor of claim 1 wherein said isolation gate is biased to a negative potential.
8. The sensor of claim 1 wherein said isolation gate is biased to provide electrical isolation between adjacent pixels.
9. The sensor of claim 1 wherein said isolation gate has an n-type conductivity.
10. The sensor of claim 9 wherein said n-type isolation gate is biased to a negative reference voltage.
11. The sensor of claim 1 wherein said isolation gate has a p-type conductivity.
12. The sensor of claim 11 wherein said p-type isolation gate is biased to a positive voltage.
13. The sensor of claim 12 wherein said positive voltage is about 5 volts or less.

14. The sensor of claim 1 wherein said isolation region comprises a trench having a depth of 5000Å or less.
15. The sensor of claim 1 wherein said isolation region does not comprise a trench.
16. The sensor of claim 1 wherein said isolation region comprises an active area.
17. The sensor of claim 1 wherein said photosensitive region comprises a photosensor.
18. The sensor of claim 1 wherein said photosensitive region comprises a photodiode.
19. The sensor of claim 1 wherein said photosensitive region comprises a photogate.
20. The sensor of claim 1 wherein said photosensitive region comprises a photoconductor.
21. The sensor of claim 1 wherein said image sensor comprises a CMOS image sensor.
22. The sensor a claim 21 wherein said CMOS image sensor comprises a three transistor (3T) CMOS image sensor.
23. The sensor of claim 21 wherein said CMOS image sensor comprises a four transistor (4T) CMOS image sensor.
24. The sensor of claim 1 wherein said image sensor comprises a CCD image sensor.
25. An image sensor, said image sensor comprising:

an active layer of a first conductivity type formed within a substrate;
at least one transistor gate formed over a portion of said active layer;
a photosensor formed adjacent to said transistor gate;
an isolation region formed in said active layer adjacent to said photosensor; and
an isolation gate formed over at least a portion of said isolation region.

26. The sensor of claim 25 wherein said photosensor comprises a p-n-p junction region formed under said at least one transistor gate, said p-n-p junction region comprising a surface layer of said first conductivity type overlying a photosensitive region of a second conductivity type, said photosensitive region overlying said active layer of said first conductivity type.
27. The sensor of claim 26 wherein said isolation region is formed in said active layer adjacent to said p-n-p junction region.
28. The sensor of claim 25 wherein said photosensor comprises a photodiode.
29. The sensor of claim 25 wherein said photosensor comprises a photogate.

30. The sensor of claim 25 wherein said photosensor comprises a photoconductor.
31. The sensor of claim 25 wherein said photosensor comprises a p-n-p diode.
32. The sensor of claim 25 wherein said photosensor comprises a buried diode.
33. The sensor of claim 25 wherein said isolation region comprises a trench having a depth of 4000Å or less.
34. The sensor of claim 25 wherein said isolation region does not comprise a trench.
35. The sensor of claim 25 wherein said isolation region comprises an active area.
36. The sensor of claim 25 wherein said transistor gate has an n-type conductivity.
37. The sensor of claim 25 wherein said isolation gate has a p-type conductivity.
38. The sensor of claim 26 wherein said isolation gate is biased to accumulate holes in a connection region formed between said p-n-p junction region and said isolation region.
39. The sensor of claim 25 wherein said isolation gate is biased to a ground potential.
40. The sensor of claim 37 wherein said isolation gate is biased to a negative voltage potential.

41. The sensor of claim 38 wherein said isolation gate is biased to a positive voltage potential.
42. The sensor of claim 25 wherein said isolation gate assists in isolating said photosensor from an adjacent active area containing another photosensor.
43. The sensor of claim 25 wherein said isolation region comprises a trench having sidewalls, said trench being filled with an insulating material.
44. The sensor of claim 43 wherein said isolation gate is biased to create positively charged holes along a sidewall of said trench.
45. The sensor of claim 25 wherein said transistor gate is a transfer gate.
46. A processor based system comprising the sensor of claim 25.
47. A CMOS image sensor comprising:
 - a pixel for receiving incident photo energy and converting it into an electrical signal;
 - said pixel comprising:
 - a photosensitive area for accumulating photo-generated charge;

a floating diffusion region adjacent a side of said
photosensitive area for receiving charge from said
photosensitive area;
a read out circuit comprising at least an output transistor for
reading out charge from said floating diffusion region;
an isolation region formed around at least a portion of said
pixel; and
an isolation gate formed over at least a portion of said
isolation region.

48. The image sensor of claim 47 wherein said isolation gate is
of a same conductivity type as a gate of said output
transistor.
49. The image sensor of claim 47 wherein said isolation gate
has an n-type conductivity.
50. The image sensor of claim 47 wherein said isolation gate
has a p-type conductivity.
51. The image sensor of claim 47 wherein said isolation gate is
biased to a ground potential.
52. The image sensor of claim 49 wherein said isolation gate is
biased to a negative potential.
53. The image sensor of claim 50 wherein said isolation gate is
biased to a positive potential.

54. The image sensor of claim 47 wherein said isolation region comprises a trench having a depth of 4000Å or less.
55. The image sensor of claim 47 wherein said isolation region does not comprise a trench.
56. The image sensor of claim 47 wherein said isolation region is an active area.
57. The image sensor of claim 47 wherein said isolation gate is formed over a substantial portion of said isolation region.
58. The image sensor of claim 47 wherein said photosensitive area comprises a photodiode.
59. The image sensor of claim 47 wherein said photosensitive area comprises a photogate.
60. The image sensor of claim 47 wherein said photosensitive area comprises a photoconductor.
61. The image sensor of claim 58 wherein said photosensitive area comprises a p-n-p diode.
62. The image sensor of claim 58 wherein said photosensitive area comprises a buried diode.
63. An image sensor comprising:
a semiconductor substrate having a plurality of image sensor pixels formed thereon;
each of said pixels comprising a photosensitive region and a floating diffusion region;

an active area formed between adjacent pixels; and
at least one isolation gate formed over a portion of said
active area.

64. The sensor of claim 63 wherein said pixel comprises at least one transistor gate for transferring photoelectric charges and wherein said isolation gate is of the same conductivity type as said at least one transistor gate.
65. The sensor of claim 63 wherein said photosensitive region comprising a p-type conductivity substrate, an n-type conductivity photodiode region, and a p-type conductivity surface region.
66. The sensor of claim 63 wherein said isolation gate is biased to ground.
67. The sensor of claim 63 wherein said isolation gate is biased to a negative potential.
68. The sensor of claim 63 wherein said isolation gate is biased to provide electrical isolation between adjacent pixels.
69. The sensor of claim 63 wherein said isolation gate has an n-type conductivity.
70. The sensor of claim 69 wherein said n-type isolation gate is biased to a negative reference voltage.
71. The sensor of claim 63 wherein said isolation gate has a p-type conductivity.

72. The sensor of claim 71 wherein said p-type isolation gate is biased to a positive voltage.
73. The sensor of claim 72 wherein said positive voltage is about 5 volts or less.
74. An integrated circuit comprising:
 - a semiconductor substrate having a plurality of image sensor pixels formed thereon;
 - each of said pixels comprising a photosensitive region and a floating diffusion region;
 - an isolation region formed between adjacent pixels;
 - at least one isolation gate formed over a portion of said isolation region, said isolation gate being biased to a constant voltage such that the isolation gate constantly reverse biases the isolation region.
75. The circuit of claim 74 wherein said isolation region comprises a trench having a depth of 4000Å or less.
76. The circuit of claim 74 wherein said isolation region does not comprise a trench.
77. The circuit of claim 74 wherein said isolation region is an active area.
78. The circuit of claim 74 wherein said isolation region comprises an insulation filled trench having sidewalls.

79. The circuit of claim 78 wherein said voltage causes holes to accumulate in a region between said photosensitive region and said sidewalls of said trench.
80. The circuit of claim 74 wherein said pixels further comprise a transfer gate between said photosensitive region and said floating diffusion region.
81. The circuit of claim 80 wherein said transfer gate and said isolation gate are of the same conductivity type.
82. The circuit of claim 74 wherein said isolation gate has an n-type conductivity.
83. The circuit of claim 74 wherein said isolation gate has a p-type conductivity.
84. The circuit of claim 74 wherein said constant voltage is a ground potential.
85. The circuit of claim 82 wherein said constant voltage is a negative potential.
86. The circuit of claim 83 wherein said constant voltage is a positive potential.
87. The circuit of claim 80 wherein said isolation gate surrounds a substantial portion of said pixels but does not contact said transfer gate or said floating diffusion region.

88. An image sensor comprising:
- a substrate having a doped layer of a first conductivity type;
 - an array of pixel sensor cells formed in said doped layer;
 - an isolation region formed between each pixel sensor cell;
 - and
 - an isolation gate formed over a substantial portion of said isolation region, said isolation gate being formed over at least a portion of said doped layer.
89. An integrated circuit comprising:
- a semiconductor substrate having an image sensor pixel formed thereon;
 - said pixel comprising at least one transfer gate disposed over and between a floating diffusion region and a photosensitive active region;
 - an isolation channel formed in said substrate and between said pixel and an adjacent pixel; and
 - an isolation gate formed over said isolation channel, whereby said isolation gate extends around substantially all of said photosensitive active region, the isolation gate being biased by a voltage such that the isolation gate biases the isolation channel.

90. The integrated circuit of claim 89 wherein the isolation region comprises a filled trench, said filled trench being less than about 0.7 microns deep.
91. The integrated circuit of claim 89 wherein said transfer gate and said isolation gate are formed of a same conductivity type.
92. The integrated circuit of claim 89 wherein said voltage is a ground potential.
93. The integrated circuit of claim 89 wherein said isolation gate is formed of an n-type conductivity material.
94. The integrated circuit of claim 89 wherein said voltage is a negative potential.
95. The integrated circuit of claim 89 wherein said isolation gate is formed of a p-type conductivity material.
96. The integrated circuit of claim 95 wherein said voltage is a positive potential.
97. The integrated circuit of claim 89 wherein said isolation gate is biased to accumulate holes in a connection region between said photosensitive active region and said isolation region.
98. A method of forming an image sensor comprising the steps of:

forming a pixel within a substrate;

forming an isolation region adjacent said pixel; and
forming an isolation gate over said isolation region and over
at least a portion of a connection region formed adjacent to
said isolation region.

99. The method of claim 98 wherein said isolation gate has the same conductivity type as at least one transistor gate of said pixel.
100. The method of claim 98 wherein a length of said isolation gate is adjusted to minimize cross talk between adjacent pixels.
101. The method of claim 98 wherein said isolation region is an active area between adjacent pixels.
102. A method of operating an image sensor, said image sensor comprising a pixel, an isolation region adjacent said pixel, and an isolation gate provided over said isolation region and adjacent to said pixel said method comprising the steps of:
forming a separation between a photodiode region of said pixel and said isolation region by applying a voltage to said isolation gate.
103. The method of claim 102 wherein said method of forming a separation comprises accumulating holes in a connection region between said photodiode region and said insulation region.

104. The method of claim 102 comprising applying a grounded potential to said isolation gate.
105. The method of claim 102 comprising applying a negative potential to said isolation gate.
106. The method of claim 102 wherein said isolation region is an active area formed between adjacent pixels.
107. A method of forming an image sensor comprising:
forming an active layer of a first conductivity type on a substrate;
forming a photosensor in said active layer; and
forming an isolation gate over at least a portion of said active layer adjacent said photosensor.
108. The method of claim 107 wherein said active layer adjacent said photosensor is an isolation region.
109. The method of claim 108 comprising forming said isolation gate over a substantial portion of said isolation region.
110. The method of claim 109 further comprising forming a length of said isolation gate to minimize cross-talk between adjacent pixels.
111. The method of claim 107 wherein forming said photosensor further comprises forming a p-n-p junction region in said active layer by forming a photo region of a second conductivity type overlying said active layer of said

first conductivity type and forming a surface layer of said

first conductivity type overlying said photo region.

112. The method of claim 107 wherein forming said photosensor comprises forming a photodiode.
113. The method of claim 107 wherein forming said photosensor comprises forming a photogate.
114. The method of claim 107 wherein forming said photosensor comprises forming a photoconductor.
115. The method of claim 107 wherein forming said photosensor comprises forming a p-n-p diode.
116. The method of claim 107 wherein forming said photosensor comprises forming a buried diode.
117. The method of claim 107 wherein said image sensor is a CCD sensor.
118. The method of claim 107 wherein said image sensor is a CMOS image sensor.
119. A method of forming a CMOS image sensor comprising:
forming a CMOS image sensor pixel within a substrate; said pixel being formed by:
forming a photosensitive area for accumulating photo-generated charge;
forming a floating diffusion region adjacent one side of said photosensitive area;

forming an output transistor for reading out charge from
said floating diffusion region;
forming a read out circuit comprising at least said output
transistor;
forming an isolation region around at least a portion of said
pixel; and
forming an isolation gate over at least a portion of said
isolation region.

120. The method of claim 119 wherein said isolation region is an active area.
121. The method of claim 120 comprising forming said isolation gate over a substantial portion of said isolation region.
122. The method of claim 121 further comprising forming a length of said isolation gate to minimize dark current in said image sensor.
123. The method of claim 119 wherein said output transistor is a transfer gate.
124. A method of operating an integrated circuit comprising:
forming a semiconductor substrate;
forming a plurality of image sensor pixels in said substrate;
interconnecting said pixels into a circuit;

forming each of said pixels such that each of said pixels comprises a photosensitive region and a floating diffusion region;
forming an isolation region between adjacent pixels;
forming at least one isolation gate over at least a portion of said isolation region;
biasing said isolation gate to a constant voltage; and
reverse biasing said isolation region by applying said constant voltage.

125. The method of claim 124 further comprising forming a length of said isolation gate to minimize cross-talk between said adjacent pixels.
126. The method of claim 124 wherein said isolation region is an active area of said substrate.